Amendments to the Claims

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A power reduction circuit, comprising:

a logic block;

a bypass line; and

at least one micro-electromechanical (MEM) switch for selectively disabling the logic block by connecting the bypass line between an input and output of the logic block.

2. (Currently Amended) The power reduction circuit of claim 1, wherein the logic block is selected from the group consisting of a latch~~es~~, memory array~~s~~, embedded memory array~~s~~, control logic, register~~s~~, application specific integrated circuit (ASIC) core~~s~~, microprocessor~~s~~, and multithreaded processor~~s~~.

3. (Currently Amended) The power reduction circuit of claim ~~2~~ 1, wherein the ~~latch~~ logic block comprises a level-sensitive scan design (LSSD) latch.

4. (Currently Amended) ~~The~~ A power reduction circuit ~~of claim 1, wherein the at least one MEM switch for selectively disabling the logic block further comprises~~ comprising:

a logic block; and

at least one micro-electromechanical (MEM) switch for selectively disabling the logic block, the at least one MEM including:

a MEM switch for ~~selectively~~ disconnecting the logic block from power; and

a MEM switch for ~~selectively~~ disconnecting the logic block from ground.

5. (Cancelled).

6. (Currently Amended) ~~The~~ A power reduction system ~~of claim 1~~, ~~further~~ comprising:

a logic block; and

at least one micro-electromechanical (MEM) switch for selectively disabling the logic block, the at least one MEM including a MEM switch for ~~selectively~~ disconnecting an output of the logic block.

7. (Currently Amended) The power reduction system of claim 1, further comprising:

a MEM switch for ~~selectively~~ disconnecting an input of the logic block.

8. (Currently Amended) A method for power reduction, comprising:

providing a logic block and a bypass line; and

selectively disabling the logic block using at least one micro-electromechanical (MEM) switch to connect the bypass line between an input and output of the logic block.

9. (Currently Amended) The method of claim 8, wherein the logic block is selected from the group consisting of a latch~~es~~, memory array~~s~~, embedded memory array~~s~~, control logic, register~~s~~, application specific integrated circuit (ASIC) core~~s~~, microprocessor~~s~~, and multithreaded processor~~s~~.

10. (Currently Amended) The method of claim 8, wherein the ~~latch~~ logic block comprises a level-sensitive scan design (LSSD) latch.

11. (Currently Amended) ~~The~~ A method for power reduction, ~~of claim 8, wherein the step of selectively disabling the logic block further comprises~~ comprising:

providing a logic block; and

selectively disabling the logic block by:

~~selectively~~ disconnecting the logic block from power using a micro-electromechanical (MEM) ~~MEM~~ switch; and

~~selectively~~ disconnecting the logic block from ground using a MEM switch.

12. (Cancelled).

13. (Currently Amended) ~~The~~ A method ~~of claim 8~~ for power reduction, ~~further~~ comprising:

providing a logic block; and

selectively disabling the logic block by ~~selectively~~ disconnecting an output of the logic block using a micro-electromechanical (MEM) ~~MEM~~ switch.

14. (Currently Amended) The method of claim 8, further comprising:

~~selectively~~ disconnecting an input of the logic block using a MEM switch.

15. (Original) A circuit, comprising:

a logic block;

a micro-electromechanical (MEM) switch for selectively disconnecting the logic block from power;

a MEM switch for selectively disconnecting the logic block from ground;

a bypass line connected between an input and output of the logic block for passing data around the logic block; and

a MEM switch for selectively disconnecting the bypass line.

16. (Currently Amended) The circuit of claim 15, wherein the logic block is selected from the group consisting of a latch~~es~~, memory array~~s~~, embedded memory array~~s~~, control logic, register~~s~~, application specific integrated circuit (ASIC) core~~s~~, microprocessor~~s~~, and multithreaded processor~~s~~.

17. (Original) The circuit of claim 15, further comprising:

a MEM switch for selectively disconnecting an output of the logic block to prevent data from appearing on the output of the logic block.

18. (Original) The circuit of claim 15, further comprising:

a MEM switch for selectively disconnecting the input of the logic block to separate the input of the logic block from preceding circuitry.

19. (Original) The circuit of claim 15, wherein, in an operational mode of the logic block, the MEM switch for selectively disconnecting the logic block from power and the MEM switch for selectively disconnecting the logic block from ground are closed to provide the logic block with power, and the MEM switch for selectively disconnecting the bypass line is open to prevent data from passing around the logic block.

20. (Original) The circuit of claim 15, wherein, in a non-operational mode of the logic block, the MEM switch for selectively disconnecting the logic block from power and the MEM switch for selectively disconnecting the logic block from ground are open, thereby disconnecting the logic block from power, and the MEM switch for selectively disconnecting the bypass line is closed, thereby allowing data to pass around the logic block.